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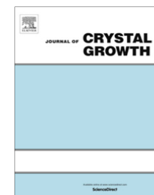

Careful stoichiometry monitoring and doping control during the tunneling interface growth of an n + InAs(Si)/p + GaSb(Si) Esaki diode

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ABSTRACT

In this work, we report on the growth of pseudomorphic and highly doped InAs(Si)/GaSb(Si) heterostructures on p-type (0 0 1)-oriented GaSb substrate and the fabrication and characterization of n+/p+ Esaki tunneling diodes. We particularly study the influence of the Molecular Beam Epitaxy shutter sequences on the structural and electrical characteristics of InAs(Si)/GaSb(Si) Esaki diodes structures. We use real time Reflection High Electron Diffraction analysis to monitor different interface stoichiometry at the tunneling interface. With Atomic Force Microscopy, X-ray diffraction and Transmission Electron Microscopy analyses, we demonstrate that an "InSb-like" interface leads to a sharp and defect-free interface exhibiting high quality InAs(Si) crystal growth contrary to the "GaAs-like" one. We then prove by means of Secondary Ion Mass Spectroscopy profiles that Si-diffusion at the interface allows the growth of highly Si-doped InAs/GaSb diodes without any III-V material deterioration. Finally, simulations are conducted to explain our electrical results where a high Band to Band Tunneling (BTBT) peak current density of $J_p = 8\ mA/\mu m^2$ is achieved.

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1. Introduction

The era of the Internet of Things (IoT) is upon us and it is clear that this will require many technology enablers incorporating large-scale-integration chips with extremely low power consumption [1]. At the transistor level, the main requirement is to achieve steep devices operating at supply voltages (V_{dd}) lower than 0.5 V to tackle the power consumption reduction challenge of future CMOS generations. One of the most promising solution till now is the use of tunnel field effect transistors (TFET) which, based on an energy filtering mechanism by Band-To-Band Tunneling (BTBT), can achieve steep subthreshold swing (SS) less than 60 mV/dec at low V_{dd} range [2]. However, even if major simulations point towards III-V based TFET as the best material option, experimental devices are still lacking behind [3]. Besides the problems encountered during any traditional FET devices (channel growth, gate stack, contacts, etc), the influence of the tunneling interface on the BTBT behavior is critical for TFET devices and remains unexplored until now. Since TFETs operate like p-n diodes in a reverse bias, we have already proposed an easy BTBT measurement method using highly doped n + $In_{0.5}Ga_{0.5}As$(Si)/p + $In_{0.5}Ga_{0.5}As$(Be) Esaki tunnel diodes to have accurate TFET predictions [4]. In the target of decreasing the tunneling length at the heterojunction, our work was extended to the staggered band gap n + $In_{0.5}Ga_{0.5}As$(Si)/p + $GaAs_{0.5}Sb_{0.5}$(Be) system where BTBT current is boosted by a factor of 60 when compared to the homojunction system [5]. The influence of doping concentration on BTBT behavior was later investigated on similar heterojunction reaching a BTBT peak current density of 1.1 $mA/\mu m^2$ [6].

In this work, we discuss the n + InAs(Si)/p + GaSb(Si) system which presents ideally a broken bandgap configuration at the tunneling heterojunction. The tunneling length with this approach is decreased due to a smaller effective band gap. This would allow a further increase in the BTBT current density and consequently an improved I_{on} in TFET devices. Since InAs and GaSb semiconductors have a small lattice mismatch (~0.6%), we show in our study the importance of a careful tunneling interface preparation during growth. We particularly investigate highly doped n + InAs(Si)/p + GaSb(Si) Esaki diodes grown with either "InSb-like" or "GaAs-like" interface transition. We demonstrate that an "InSb-like" interface is crucial for high quality subsequent InAs growth on GaSb. Using Si vapor phase doping (VPD) like process at the InAs-GaSb interface, we prove that high p + GaSb(Si) doping can be achieved without any crystalline degradation. Device

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simulations of n + InAs(Si)/p + GaSb(Si) Esaki diodes are finally performed to explain the obtained electrical characterizations and they confirm the high quality of the InAs(Si)/GaSb(Si) tunneling interface.

2. Experimental

In this study, we discuss two different n + InAs(Si)/p + GaSb(Si) heterostructures (samples A and B) grown on p-doped (0 0 1) GaSb substrates. The heteroepitaxy is performed using a III–V Riber MBE 49 chamber equipped with As and Sb valved cracker cells. Antimony and Arsenic are cracked at 900 °C to generate Sb_2 and As_2, respectively. Double-filament effusion cells are used for Ga and In metals evaporation while a mono-filament effusion cell is used for Si doping. The exact growth rate of individual In, Ga, Sb_2 and As_2 molecular beams are calibrated independently by Reflection High Energy Electron Diffraction (RHEED) oscillations on (0 0 1) InAs, GaAs and GaSb substrates. Typical growth rate of 0.5 ML/s is used for both GaSb and InAs epitaxy. Before growth, the GaSb substrate outgassing is performed under Sb_2 flux at 590 °C. The temperature is then rapidly reduced to 500 °C for the growth of a 600-nm-thick Si-doped GaSb ($\sim 1.5 \times 10^{19}/cm^3$) (extracted by Hall measurements) layer exhibiting an Sb-rich (1×3) RHEED pattern during the epitaxy. After the p-doped GaSb(Si) growth, the sample temperature is further decreased down to 450 °C under Sb flux. It is important to mention that during this temperature decrease step, the GaSb surface remains exposed to the Si doping flux to promote Si-diffusion in the p + GaSb(Si) top layer similarly to the vapor

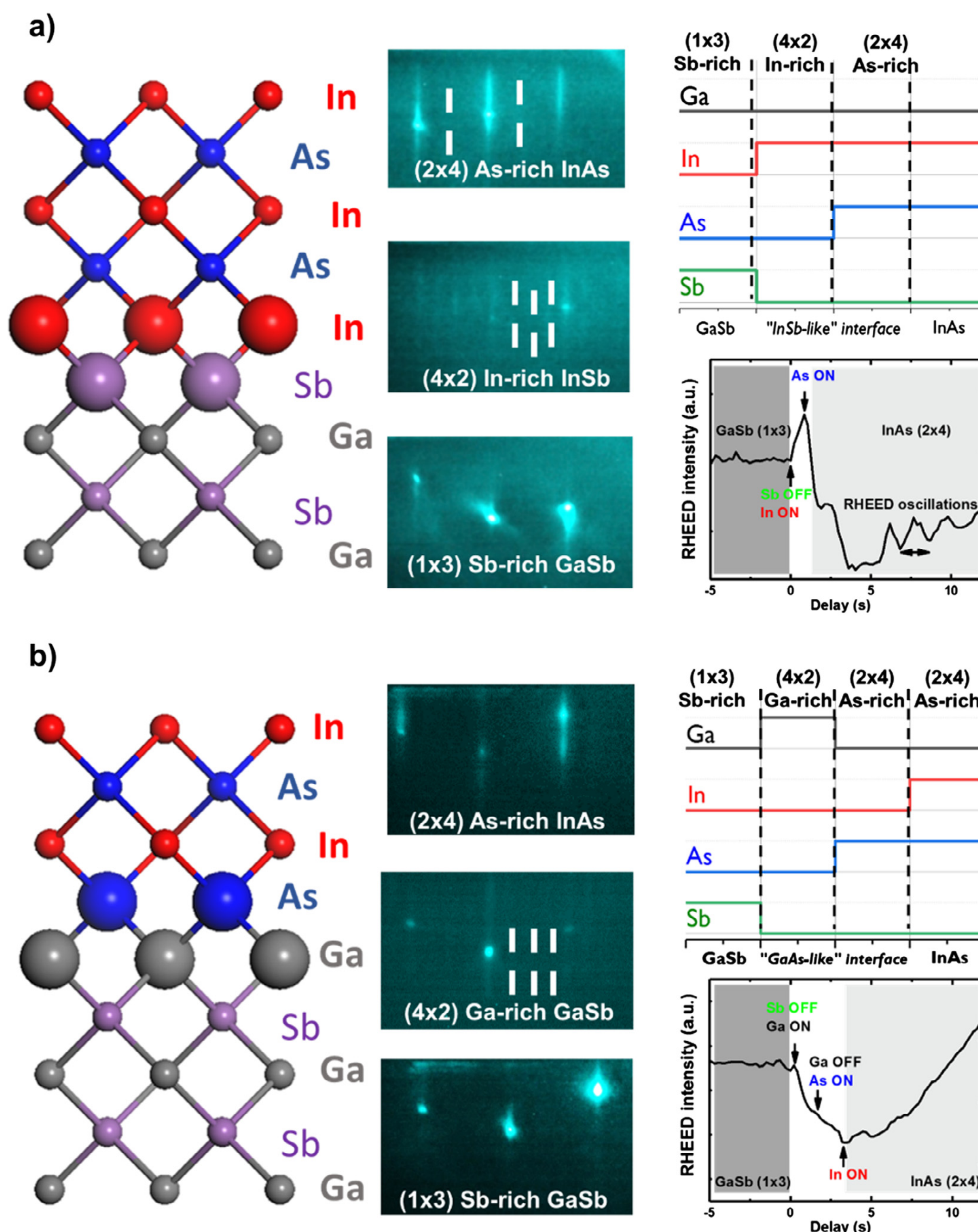

Fig. 1. Reflection High Energy Electron Diffraction (RHEED) images and MBE shutter sequence at the InAs/GaSb interface stage growth with (a) InSb-like stoichiometry and (b) GaAs-like stoichiometry. The graphs on the images present the RHEED intensity in function of the growth time during the interface transition.

phase doping process (VPD) [7]. Since high *in-situ* doping (>5.10^{19}/cm^3) into III-V layers can be challenging (either by saturation or compensation effects [8] or by degrading the crystalline quality [9]), we hope by this technique to reach a very high active Si doping levels (>7.10^{19}/cm^3) in the p + GaSb(Si) layer without any material degradation.

3. Results and discussions

Prior to the 50 nm n + doped InAs(Si) (~2 × 10^{19}/cm^3) growth, different shutter transitions are used between samples A and B as depicted respectively on Fig. 1(a) and 1(b). For both interfaces, the evolution of the RHEED patterns along the [1 1 0] direction is shown. The graphs on each figure present the RHEED intensity behavior during each interface transition. The "InSb-like" interface from sample A is obtained by closing the Sb shutter after stabilizing the temperature at 450 °C and opening the In shutter for 1 ML of In deposition where a RHEED evolution to an In-rich (4 × 2) surface reconstruction is observed. The As shutter is then immediately opened accompanied with a RHEED transition towards an As-rich (2 × 4) InAs surface reconstruction for the rest of the Si-doped InAs growth. Interestingly, clear RHEED oscillations are observed at the first stage of the InAs growth attesting a 2D layer-by-layer growth type and a very sharp interface. The extracted growth rate from these oscillations is equal to 0.5 ML/s which also matches with our In growth rate calibration.

The "GaAs-like" interface of sample B is obtained by closing the Sb shutter and opening the Ga one at the same time after the temperature stabilization at 450 °C. This results in a switch of the RHEED pattern from an (1 × 3) Sb-rich GaSb surface to a blurry Ga-rich (4 × 2) surface reconstruction. Contrary to the InSb-like case, the RHEED intensity at this stage decreases instantly indicating a more 3D island growth type. Ga shutter is then directly closed and Arsenic is sent to the surface leading to the appearance of an As-rich (2 × 4) surface reconstruction. The In shutter is then opened for the rest of the 50 nm Si-doped InAs growth and the RHEED intensity re-increases due to the layer smoothing but with the absence of clear RHEED oscillations.

Fig. 2(a) and (b) display the surfaces respectively from samples A and B, measured by AFM for (1 × 1) μm^2 scanning area. From the AFM analyses, the advantage of the "InSb-like" interface (sample A), which exhibits step and terrace surface morphology with a low RMS roughness of 0.2 nm, is obvious as compared to the "GaAs-like" interface (sample B) where pits are observed on the surface and a high RMS roughness of 4.2 nm. The ω-scans of the InAs (0 0 4) Bragg reflections for both the interface nature samples, used as a quality criterion for the InAs crystalline perfection, are presented on Fig. 2(c). Surprisingly, the extracted Full Width of Half Maximum (FWHM) of InAs (0 0 4) reflections from both "InSb-like" and "GaAs-like" samples are extremely small around ~11.8 arcsec. However, the crystalline quality difference between both interfaces is highlighted in the strong mosaicity visible in the bottom area of the "GaAs-like" interface spectrum. The Q factor which is defined as (Area of crystal part/Area of mosaic part) is calculated to be 57 for sample A (InSb-like interface) versus 1.6 for sample B (GaAs-like interface). The origin of this mosaicity is attributed to the formation of a very low density of 60° misfit dislocations formed at the heterostructure GaSb/InAs interface [10]. This indicates that the use of a "GaAs-like" interface promotes the formation of a very low density of 60° MDs at the InAs/GaSb tunneling interface which is not present in the case of the "InSb-like" interface. These XRD characterizations are in good agreement with the extracted surface roughness as measured by AFM.

To further assess the interface quality, the cross-section Transmission Electron Microscope (TEM) analyses of samples A and B are shown on Fig. 3. High-Angle Annular Dark Field (HAADF)-STEM images on Fig. 3(a) and (b) from samples A and B respectively indicate a very flat surface with the absence of structural defects (like pinholes, etch pits, etc) for the "InSb-like" interface option, while pits formed in the InAs layer are clearly visible for the "GaAs-like" interface which are the origin of the strong roughening measured by AFM. The high-resolution (HR-STEM) images on Fig. 3(c) and (d) attest on the sharp InAs/GaSb interface for sample A, however a rougher and darker region visible at the interface from sample B compared to sample A and indicating a much higher strain difference induced by the "GaAs-like" interface. All these observations are in agreement with previous reports on similar InAs/(Al,Ga)Sb systems [11] which shows that a "GaAs-like" interface character induces tensile strain and partial relaxation which degrades the subsequent InAs growth whereas the compressed "InSb-like" interface nature promotes a compressive strain compensation preventing InAs crystal degradation. The HR-HAADF-STEM images of "InSb-like" and "GaAs-like" interfaces, along the ⟨1 1 0⟩ direction, are depicted on Fig. 3(e) and (f), respectively.

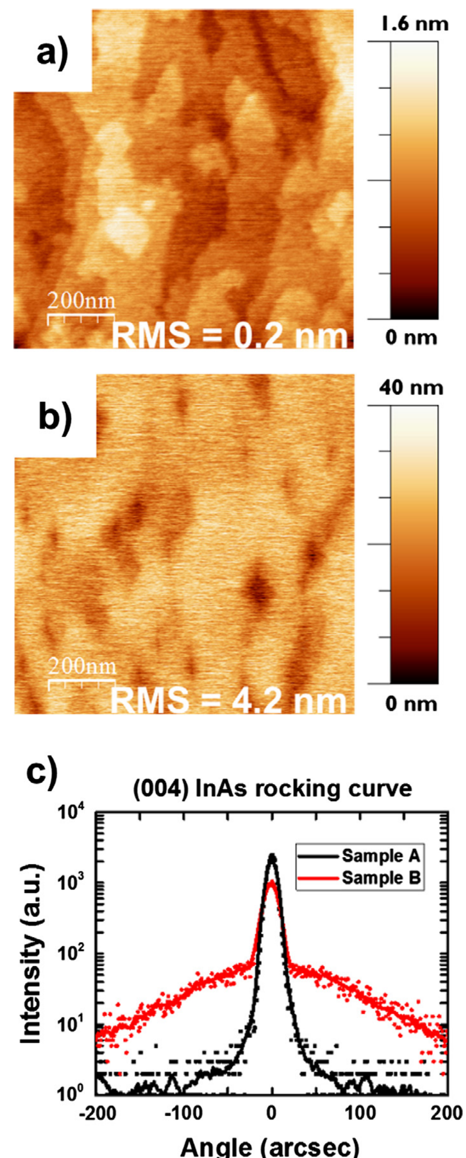

Fig. 2. (a) and (b) Atomic Force microscopy images of InAs(Si) grown on GaSb(Si) with InSb-like (sample A) and GaAs-like (sample B) interfaces, respectively. (c) The comparison between the two samples of the (0 0 4) ω scans diffraction peaks ω_{InAs} = 31.25°.

Since the brightness of each column is proportional to the square of the atomic number (Z^2), the intensity profiles can enable us to identify the exact atomic arrangement for both interfaces. For sample A, the intensity profiles demonstrate the presence of exactly 1ML of InSb at the InAs/GaSb interface with a very sharp transition. On the other hand, the intensity profiles for sample B indicate the "GaAs-like" atomic arrangement at the interface. These TEM observations not only confirm the different interface natures between the two samples but also highlight the MBE for careful interface monitoring. Furthermore, it shows the ability of the TEM technique as a suitable characterization tool for accurate interface observations at the ML level.

The Esaki diodes with vertical nanowire architecture are fabricated according to the device process flow described in Ref. [4].

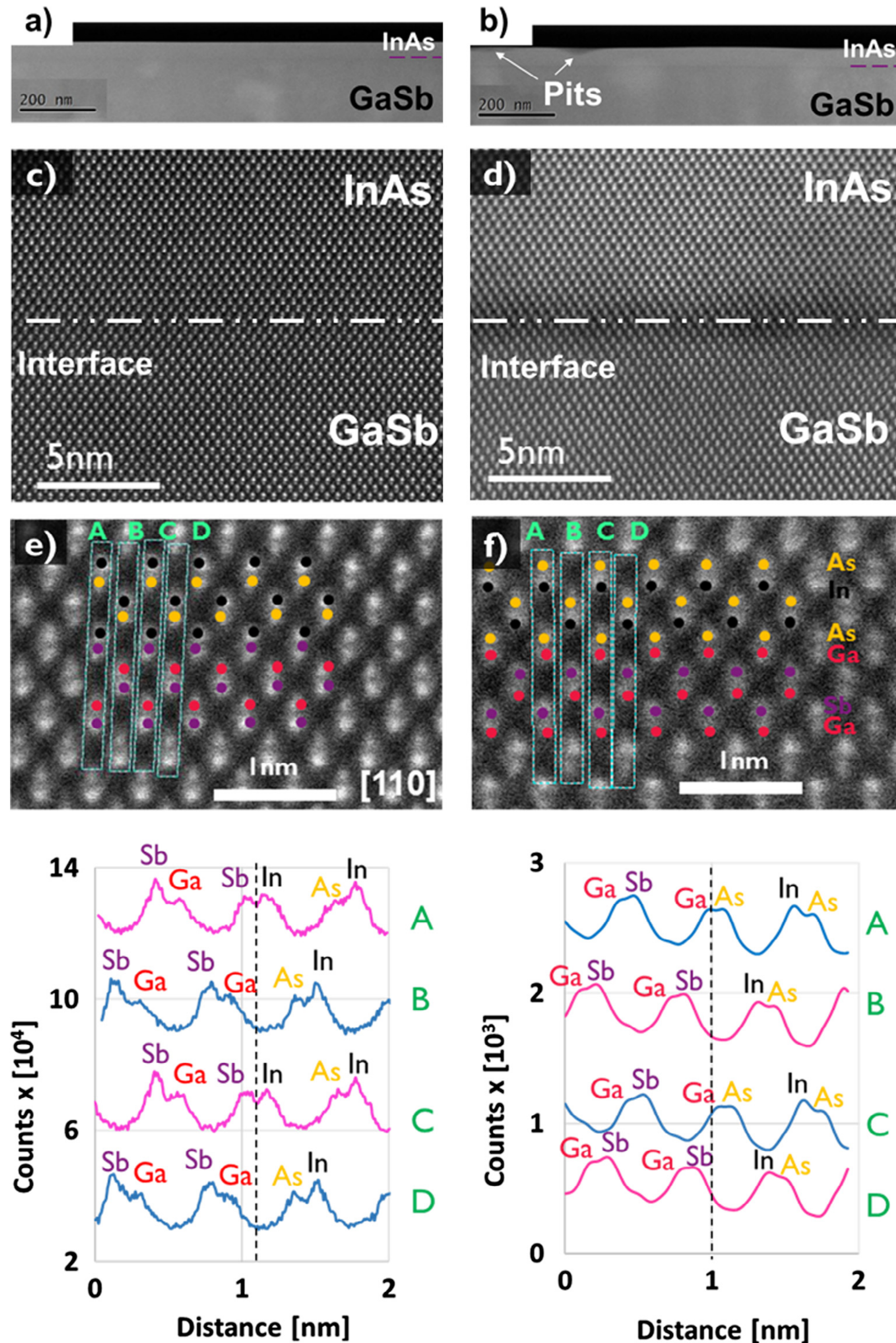

Fig. 3. High-angle annular dark field (HAADF) STEM images of sample A (a) and sample B (b) at the InAs/GaSb interfaces. (c) High-Resolution STEM image of sample A interface exhibiting a sharp InAs/GaSb interface whereas for sample B (d) the overall brightness is reduced over a wider interface region due to stress that influences the channeling contribution to the contrast. HR-HAADF-STEM images of the InSb-like (e) and GaAs-like (f) interface along with the intensity traces at the interface region showing the right distribution of atoms along the heterointerface.

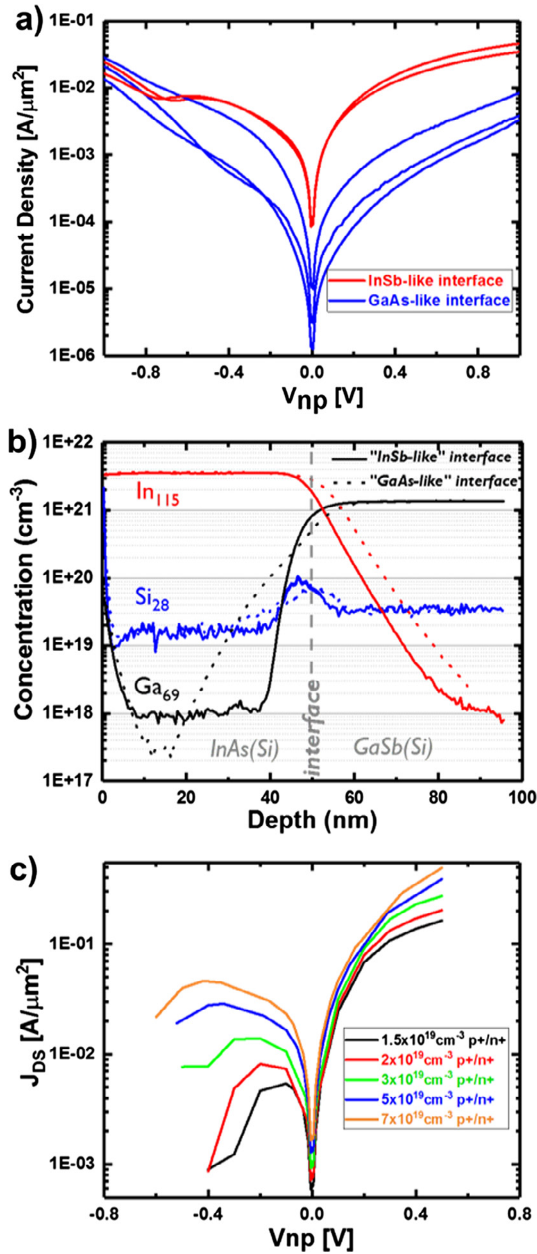

Fig. 4. (a) J–V characteristics of the n + InAs(Si)/p + GaSb(Si) Esaki diodes with different interface stoichiometry at RT. (b) SIMS analysis of samples A and B (InSb-like and GaAs-like interfaces, respectively) showing high doping concentration at the interface level due to careful Si-diffusion control. (c) Device simulations on the expected impact of increasing doping level in source and drain of a pn-diode. The simulator used to obtain the I-V curves is a semi-classical simulator, which self-consistently solves the Poisson- and drift-diffusion equations with a non-local BTBT model [16].

The nanowires diameter presented here are around 100 nm. Fig. 4 (a) shows the current density (J) versus voltage characteristics of the two Esaki diodes with either InSb (red line) or GaAs (blue line) interfaces.[1] There is a noticeable variability in the J-V characteristics of the devices so several device characteristics are plotted for each sample. For the "InSb-like" interface, dominant BTBT current is observed where negative differential resistance (NDR) is shown in forward bias ($V_{np} < 0$) with an average BTBT peak current density of Jp = 8 mA/μm^2. On the other hand, "GaAs-like" interface shows no NDR obviously due to a degraded InAs/GaSb tunneling interface. Similar observations on the influence of dislocations coming from mismatched growth of the active layer with the substrate on the I-V characteristics have been reported elsewhere [12–15]. However, the peak current in our diodes exhibits a higher value and a more negative forward bias than what is expected from a n + InAs/p + Ga Sb Esaki diode with a n + doping of ~2 × 10^{19}/cm^3 and p + doping of ~1.5 × 10^{19}/cm^3 [16]. To understand this behavior, the SIMS profiles of samples A and B interfaces are presented on Fig. 4(b). One can notice that the ascendant Ga profile of sample A is much steeper than the one of sample B, which is another indication of a rougher interface with the GaAs-like case. Indium profiles tailing slopes are more difficult to compare as they are more limited by SIMS artefacts (beam-induced mixing + knock-on) but one can still notice a steeper decrease in sample A compared to sample B (around 9 and 11 nm/decade, respectively). Si concentrations extracted by SIMS in both the GaSb and InAs layers are identical to the active concentrations measured by Hall characterization on our calibrated samples InAs (Si)/SI-InP and GaSb(Si)/SI-GaAs, respectively. Interestingly, a very high Si-doping concentration peak (~9 × 10^{19}/cm^3) is observed at the interface of both samples which is obviously due to the Si vapor phase doping process which induces Si diffusing into the GaSb top layer. Even if it's difficult to have an accurate value of the Si active dopants at the tunneling interface, these results along with the above AFM and TEM analyses show the effectiveness of our diffusion technique to reach very high Si doping concentrations at the tunneling interface without any III-V material degradation.

To illustrate the peak current behavior upon increasing the doping level, the expected impact of increasing doping level in source and drain of a n + InAs/p + GaSb diode is shown on Fig. 4(c). It's important to mention that many aspects are not included in these simulations like strain and doping-dependent bandgap-narrowing, hence an exact match with the experiment is not to be expected. The simulator used to obtain the J-V curves is a semi-classical simulator, which self-consistently solves the Poisson- and drift-diffusion equations with a non-local BTBT model [17]. The diode architecture consists of p-doped and n-doped regions both with the same doping level (see legend of Fig. 4c). It can be observed, that the reverse bias BTBT-dominated current steadily increases with doping. This is due to a steady increase in E-field and corresponding decrease in tunnel path length, as well as a steady increase in tunneling window due to the increased doping degeneracy. In forward bias, the NDR peak voltage steadily increases while the forward bias at which the NDR peak occurs also steadily increases (in absolute value). The latter is the result of the increasing doping degeneracy, resulting in a more negative forward bias to turn off the BTBT current, hence a shift of all features to more negative forward biases.

4. Conclusion

In summary, we have presented a detailed study on a n + InAs/p + GaSb Esaki diodes reporting high BTBT peak current density Jp = 8 mA/μm^2 linked to the high Si-doping level at the heterojunction. We have particularly shown that sharp interfaces at the monolayer (ML) level can be obtained by careful RHEED analysis of the surface reconstruction transitions. Our AFM, XRD and TEM results conclude that an "InSb-like" tunneling interface stoichiometry is essential in order to achieve high quality n + InAs/p + GaSb crystal growth. The electrical results of the fabricated diodes along with the corresponding SIMS profiles demonstrate that Si-diffusion at the interface allow the growth of highly doped InAs/GaSb diodes without any material deterioration. Since peak current densities are usually related to drive current in TFETs, these diodes show

[1] For interpretation of color in Fig. 4, the reader is referred to the web version of this article.

the promise to further boost I_{ON} in TFETs. The growth of this system onto commercially available substrates [18] along with the right NW digital etching [19] will further push the CMOS technology roadmap through III-V NW TFET devices onto Si substrates.

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